In the Specification

Applicant presents replacement paragraphs below indicating the changes with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing.

Please add a new paragraph at line 2, page 1 after the title as follows:

Cross Reference to Related Application

This application is a continuation of application Serial No. PCT/EP00/00990, filed February 8, 2000.

Please add the section heading before line 3, page 1 as follows:

Field of the Invention

Please add the section heading before line 8, page 1 as follows:

Background of the invention

Please add the section heading before line 1, page 2 as follows:

Summary of the Invention

Please add the section heading before line 32, page 8 as follows:

Brief Description of the Drawings

Please add the section heading before line 20, page 9 as follows:

Detailed Description

Please replace the paragraph at line 7, page 11 as follows:

According to the principles of the first and second preferred embodiment of the invention, receiving arrangements 7, ~~71~~ 7' as shown in FIG. 2 and 3, receive a digital transport stream signal suitable for being transmitted to a satellite and output a first and a second digital output signal 0 and 0'. These signals are input into processing means 8, 8' which trace the predetermined bit sequence or group of bit sequences in said first and said second digital output

signals and determine the delay between the first and second digital output signals on the basis of said tracing of the bit sequence or group of bit sequences. Each of the receiving arrangements 7, ~~71~~ 7' comprises a tuner 71, 71', demodulator 72, 72', and a decoder 73, 73'. The processing means 8, 8' performs the tracing operation on bit level although the bit stream processed by the processing means 8, ~~81~~ 8' may vary.

Please replace the paragraph at line 26, page 12 as follows:

The stop signal STOP is generated by a second processor ~~81~~ 8' receiving a digital output signal 0 from a second receiving/decoding arrangement 7' which comprises a second tuner ~~711~~ 71', a second QPSK demodulator 72' and a second decoder 73'. The first and second receiving/decoding arrangements 7 and 7' are identical regarding their structure and components. The input signal to the second receiving/decoding arrangement ~~71~~ 7' is supplied from a downconverter 10 which receives a signal from the satellite antenna 5 and which comprises all the equipment necessary to convert the received signal from the satellite antenna 5 into a signal corresponding to the output signal of the QPSK modulator 3. However, as the signal has ~~traveled~~ travelled from the satellite antenna 5 to the satellite and back, the received signal is delayed. Apart from the delay the digital output signal 0 of the second decoding arrangement ~~71~~ 7' is identical to the digital output signal of the first decoding arrangement 7 if receiving/decoding arrangements 7, ~~71~~ 7' having identical structure and components are provided.

Please replace the paragraph at line 12, page 13 as follows:

For generating the stop signal STOP the second processor ~~81~~ 8' traces the predetermined bit sequence or group of bit sequences in the digital output signal ~~01~~ 0' of the second receiving/decoding arrangement 7'. Upon detection of the predetermined bit sequence or group of bit sequences the second processor 8' sends the stop signal STOP to the time measurement circuit 9 which stops the time measurement. The measured time corresponds to the distance between the ground station 5 and the satellite.

Please replace the paragraph at line 22, page 13 as follows:

As two identical receiving/decoding arrangements 7 and ~~71~~ 7' are provided the measured time corresponds to the delay between the transmitted signal and the received signal introduced by the signal travel path from the satellite antenna to the satellite and back. Therefore, the distance between the ground station and the satellite can be determined on the basis of the measured time. Delays introduced by the components of the receiving/decoding arrangements can be neglected as the same delay is introduced by the first and by the second receiving/decoding arrangement. The influence of the upconverter 4 and of the downconverter 10 can be taken into account as the delay introduced thereby can easily measured with other measurement equipment, i.e. is known.

Please replace the paragraph at line 4, page 16 as follows:

Furthermore, FIG. 3 shows an second ground station 12 comprising a second satellite antenna 13 and a downconverter ~~101~~ 10' which receives a signal from the second satellite antenna 13 and which comprises all the equipment necessary to convert the received signal from the satellite antenna 13 into a signal corresponding to the output signal of the QPSK modulator 3. However, as the signal has ~~traveled~~ travelled from the first satellite antenna 5 via the satellite to the second satellite antenna 13, the received signal is delayed.

Please replace the paragraph at line 25, page 13 as follows:

The second processor 8' receives the digital output signal 0' of the second receiving/decoding arrangement 7' and traces the predetermined bit sequence or group of bit sequences. Upon detection of the predetermined bit sequence or group of bit sequences the second processor 8' sends a second trigger signal RECEPTION to a time measurement circuit 9' which registers the time stamp information supplied (the reception time) by a second clock circuit ~~111~~ 11' at this instant.

Please replace the paragraph at line 5, page 22 as follows:

The stop signal STOP is generated by a second processor ~~81~~ 8' receiving an output signal from a second receiving arrangement 7' which consists of a second tuner 700'. The first and

second tuner 700 and 700' are identical regarding their structure and components. The input signal to the second tuner 700' is supplied from a downconverter 10 which receives a signal from the satellite antenna 5 and which comprises all the equipment necessary to convert the received signal from the satellite antenna 5 into a signal corresponding to the output signal of the QPSK modulator 3. However, as the signal has ~~traveled~~ travelled from the satellite antenna 5 to the satellite and back, the received signal is delayed. Apart from the delay the output signal of the second tuner 700' is, for the purposes of the invention, identical to the output signal of the first tuner 700.

Please replace the paragraph at line 32, page 22 as follows:

As two identical receiving arrangements 7 and 7', i.e. the first and second tuner 700 and 700', are provided the measured time corresponds to the delay between the transmitted-signal and the received signal introduced by the signal travel path from the satellite antenna to the satellite and back. Therefore, the distance between the ground station and the satellite can be determined on the basis of the measured time. Delays introduced by the components of the tuners can be neglected as the same delay is introduced by the first and by the second tuner. The influence of the upconverter 4 and of the downconverter 10 can be ~~take~~ taken into account as the delay introduced thereby can easily measured with other measurement equipment, i.e. is known.

Please replace the paragraph at line 13, page 23 as follows:

As described above, the processors 8 and 8' are arranged to determine a signal pattern in the tuner output signal based on a predetermined bit sequence or group of bit sequences and the known processing in the multiplexer/encoder 2 and the QPSK modulator 3. Alternatively, the first processor 8 may be set up to start the sampling/storing operation at any time to obtain a series of stored values corresponding to the first tuner output signal during the sampling/storing operation. Similarly, the second processor 8' may be set up to start the sampling/storing operation at a corresponding time to obtain a series of stored values corresponding to the second tuner output signal during the sampling/storing operation. The stored sample value series are compared to trace a match or correlation which is indicative of the time delay introduced into the signal by the traveling to the satellite and back. It should be noted that the storage requirements

in the second processor ~~81~~ 8' may be reduced if the sampling/storing operation is started only after a time which is almost equal but less than the expected delay of the signal. This alternative of the third embodiment also allows to combine the first and second processor into a single processing means avoiding the need for a time measurement circuit 9 since the delay can-be determined on the basis of the sampling frequency used in the sampling operation.

Please replace the paragraph at line 29, page 30 as follows:

In the reference station 100 and/or the receiving station 106 an extracting means 108, 108' is provided which extracts the counter value CNT from the received signal, i.e. separates the counter values CNT from the digital data stream DS. The extracted (separated) counter value CNT is used to control a replica counting means 109 in the reference station 100 and/or a replica counting means ~~1091~~ 109' in the receiving station 106. An additional timing means, for example a clock, (not shown in Fig.6) may be used for supplying a driving signal to the replica counter means 109, 109' such that the extracted (separated) counter value CNT is sufficient for controlling the replica counter means 109, 109' at the times when the counter value CNT is extracted (separated) from the received signal, i.e. digital data stream DS. In the case of the ground station 100 the reference timing means 101 may be used instead of an additional timing means. This approach is advantageous as no further clock synchronization is required since a single clock is used. In the case of the receiving station 106 additional timing means should be provided.